CLAIMS

We Claim:

1. A method used in a display system that comprises an array of micromirrors, each micromirror being associated with one or more memory cell of a memory cell array, to produce images, the method comprising:

loading a pixel data matrix of the image;

delivering the rows of the matrix in parallel into a data converter;

transposing, by the data converter, the pixel data matrix into a bitplane matrix following a bitplane format wherein matrix elements in one row of the matrix represent one pixel of the image; and

sending the bitplane matrix into the memory cell array for actuating the micromirrors such that the image is produced by the micromirrors.

2. The method of claim 1, wherein the matrix elements in one column of the matrix represent one pixel of the image.

3. The method of claim 1, wherein the step of transposing the pixel data matrix into the bitplane matrix further comprises:

delaying the pixel data of the matrix according to a sequence of time-units such that a pixel data at column i and row j is delayed j time-units relative to the data element at column i and row 1 and one time-unit relative to the data element at column i+1 and row j;

shifting the delayed data elements at each time-unit of the sequence of time-units according to a shifting rule, wherein the shifting rule states that: for a matrix having m columns and n rows,

a) the data element of row j at the k^{th} time-unit of the time-unit sequence is shifted to row j-1 at the same time-unit; and the data element at row 1 of the k^{th} time-unit is shifted to row m at the same time-unit, wherein k runs from 1 to m+n time-units; and

b) the data elements at the n^{th} and m^{th} time-unit are not shifted; and

delaying the shifted data elements of the matrix according to the sequence of time-units such that a pixel data of row j at time-unit p is delayed j time-units relative to the data element of row j-1 at time-unit p.

4. The method of claim 2, wherein the step of shifting the delayed data elements further comprises:

loading the shifted data elements at each time-unit into a register of the data converter, the register having n bits; and

sequentially shifting the loaded data elements such that the data element at bit b is shifted to bit $b+1$, and the data element at bit n is shifted to the first bit of the register.

5. The method claim 1, wherein the value of the data element of the matrix determines the voltage of a memory cell of the memory cell array, and the location of the matrix element in a column of the matrix determines the duration of the voltage in the memory cell, such that the micromirror associated with said memory cell is turned on or off for the duration of said voltage.

6. The method of claim 1, wherein the step of sending the bitplane matrix into the memory cell array further comprises:

loading each row of the memory cells of the memory cell array with at least a portion of a row of data elements of the transposed pixel data matrix.

7. The method of claim 1, wherein the pixel data matrix is a square matrix having $m \times m$ data elements, wherein m equals 2^n and n is an integer greater than 1.

8. The method of claim 7, further comprising:

a) transforming the pixel data matrix into a block matrix having 2×2 first order blocks, each first order block having 2×2 second order blocks, each second order block having 2×2 third order blocks, each k^{th} order block having 2×2 $(k+1)^{th}$ order blocks, and the $(n-1)^{th}$ order block having 2×2 pixel data elements;

b) transposing the pixel data matrix based on the first order blocks;

c) transposing the pixel data matrix based on the k^{th} order blocks after consecutive transposes of the pixel data matrix based on the first order block through the $(k-1)^{th}$ order blocks; and

c) transposing the pixel data matrix based on the $(n\text{-}1)^{th}$ order blocks, each of which has 2×2 pixel data elements;

9. The method of claim 7, further comprising:

a) transforming the pixel data matrix into a block matrix having 2×2 first order blocks, each first order block having 2×2 second order blocks, each second order block having 2×2 third order blocks, each k^{th} order block having 2×2 $(k+1)^{th}$ order blocks, and the $(n\text{-}1)^{th}$ order block having 2×2 pixel data elements;

b) transposing the pixel data matrix based on the $(n\text{-}1)^{th}$ order blocks, each of which has 2×2 pixel data elements;

c) transposing the pixel data matrix based on the k^{th} order blocks after consecutively transposes of the pixel data matrix based on the $(n\text{-}1)^{th}$ order block through the $(k+1)^{th}$ order blocks; and

d) transposing the pixel data matrix based on the first order blocks.

10. The method of claim 9, wherein the step of transposing the pixel data matrix based on the $(n\text{-}1)^{th}$ order blocks, each of which has 2×2 pixel data elements, further comprises:

for each $(n\text{-}1)^{th}$ order block having 2×2 pixel data elements,

delaying the data elements in the second row of the block one time-unit relative to the data elements in the first row of the block, and the data elements in the first column in each row one time-unit relative to the data elements in the second column of the same row;

shifting the delayed data elements at each time-unit;

delaying the shifted data elements in the first row of the block one time-unit relative to the data elements in the second row of the block.

11. The method of claim 9, wherein the step of transposing the pixel data matrix based on the first order block further comprises:

delaying the data elements of the matrix according to a sequence of time-units such that: a) data elements of rows 1 through $n/2$ are not delayed; b) for data elements of rows from $n/2+1$ through n, data elements at column i and row j is delayed one time-units relative

to the data element at column i+1 and row j, and is delayed $n/2$ time-units relative to the data element at the same column and the first row;

shifting the delayed data elements according to a shifting rule, wherein the shifting rule states that: at each time-unit,

a) exchanging the data element of row 1 with the data element of row ($n/2$ +1) at the time-unit; and

b) exchanging the data element of row i with the data element of row ($n/2+i$); and

delaying the shifted data elements according to the sequence of time-units such that: a) data elements of rows $n/2$+1 through n are not delayed; b) for data elements of rows from 1 through n/2, data elements at column i and row j is delayed one time-units relative to the data element at column i+1 and row j, and is delayed $n/2$ time-units relative to the data element at the same column and the first row.

12. The method of claim 1, wherein the pixel data matrix having $m \times n$ data elements and wherein m is larger than n; and wherein the step of transposing further comprises:

appending (m-n) rows to the matrix, wherein each appended row has m elements; and

after transposing the matrix with the appended rows, truncating (m-n) data elements from each row of the transposed matrix.

13. The method of claim 1, wherein the pixel data matrix having $m \times n$ data elements and wherein m is smaller than n; and wherein the step of transposing further comprises:

appending (m-n) data elements to each row of the matrix; and

after transposing the matrix with the appended rows, truncating (m-n) rows from the transposed matrix.

14. The method of claim 1, wherein the pixel data matrix is a square matrix having $m \times m$ data elements, wherein m is an integer greater than 1.

15. A method used in a display system that comprises an array of micromirrors, each micromirror being associated with a memory cell of a memory cell array, to produce images, the method comprising:

delivering a pixel data matrix of the image to a data converter such that the rows of the pixel data matrix are delivered in parallel into the data converter, wherein the pixel data matrix following a pixel data format;

delaying the data elements of the matrix according to a sequence of time-units such that a pixel data at column i and row j is delayed j time-units relative to the data at column i and the first row and one time-unit relative to the data element at column i+1 and row j;

shifting the delayed data elements at each time-unit of the sequence of time-units according to a shifting rule, wherein the shifting rule states that: for a matrix having m columns and n rows,

a) the data element of row j at the k^{th} time-unit of the time-unit sequence is shifted to row j-1 at the same time-unit; and the data element at the first row of the k^{th} time-unit is shifted to row m at the same time-unit, wherein k runs from 1 to $m+n$ time-units; and

b) the data elements at the n^{th} and m^{th} time-units are not shifted; and

delaying the shifted data elements according to the sequence of time-units such that a data element of row j at time-unit p is delayed j time-units relative to the data element of row j-1 at time-unit p.

16. The method of claim 15, wherein the pixel data matrix is a rectangular matrix.

17. The method of claim 15, further comprises:

sending the shifted and delayed data matrix into the memory cell array for actuating the micromirrors for producing the image.

18. The method of claim 17, wherein the value of the data element of the matrix determines the voltage of a memory cell of the memory cell array, and the location of the data element at the matrix determines the duration of the voltage in the memory cell, such that the micromirror associated with said memory cell is turned on or off for the duration of said voltage in said memory cell.

19. A method used in a display system that comprises an array of micromirrors, each micromirror being associated with a memory cell of a memory cell array, to produce images, the method comprising:

delivering a pixel data matrix of the image to a data converter such that the rows of the pixel data matrix are delivered in parallel into the data converter, wherein the pixel data matrix following a pixel data format;

transforming the pixel data matrix into a block matrix having 2×2 first order blocks, each first order block having 2×2 second order blocks, each second order block having 2×2 third order blocks, each k^{th} order block having 2×2 $(k+1)^{th}$ order blocks, and the $(n-1)^{th}$ order block having 2×2 pixel data elements;

transposing the pixel data matrix based on the $(n-1)^{th}$ order blocks, each of which has 2×2 pixel data elements;

transposing the pixel data matrix based on the k^{th} order blocks after consecutively transposes of the pixel data matrix based on the $(n-1)^{th}$ order block through the $(k+1)^{th}$ order blocks; and

transposing the pixel data matrix based on the first order blocks.

20. The method of claim 19, wherein the step of transposing the pixel data matrix based on the $(n-1)^{th}$ order blocks, each of which has 2×2 pixel data elements, further comprises:

for each $(n-1)^{th}$ order block having 2×2 pixel data elements,

delaying the data elements in the second row of the block one time-unit relative to the data elements in the first row of the block, and the data elements in the first column in each row one time-unit relative to the data elements in the second column of the same row;

shifting the delayed data elements at each time-unit;

delaying the shifted data elements in the first row of the block one time-unit relative to the data elements in the second row of the block.

21. The method of claim 19, wherein the step of transposing the pixel data matrix based on the first order block further comprises:

delaying the data elements of the matrix according to a sequence of time-units such that: a) data elements of rows 1 through $n/2$ are not delayed; b) for data elements of rows

from $n/2+1$ through n, data elements at column i and row j is delayed one time-units relative to the data element at column $i+1$ and row j, and is delayed $n/2$ time-units relative to the data element at the same column and the first row;

shifting the delayed data elements according to a shifting rule, wherein the shifting rule states that: at each time-unit,

a) exchanging the data element of row 1 with the data element of row $(n/2+1)$ at the time-unit; and

b) exchanging the data element of row i with the data element of row $(n/2+i)$; and

delaying the shifted data elements according to the sequence of time-units such that: a) data elements of rows $n/2+1$ through n are not delayed; b) for data elements of rows from 1 through $n/2$, data elements at column i and row j is delayed one time-units relative to the data element at column $i+1$ and row j, and is delayed $n/2$ time-units relative to the data element at the same column and the first row.

22. The method of claim 19, wherein the pixel data matrix having $m \times n$ data elements and wherein m is larger than n; and wherein the step of transposing further comprises:

appending $(m-n)$ rows to the matrix, wherein each appended row has m elements; and

after transposing the matrix with the appended rows, truncating $(m-n)$ data elements from each row of the transposed matrix.

23. The method of claim 19, wherein the pixel data matrix having $m \times n$ data elements and wherein m is smaller than n; and wherein the step of transposing further comprises:

appending $(m-n)$ data elements to each row of the matrix; and

after transposing the matrix with the appended rows, truncating $(m-n)$ rows from the transposed matrix.

24. The method of claim 19, wherein the pixel data matrix is a square matrix having $m \times m$ data elements, wherein m is an integer greater than 1.

25. The method of claim 19, wherein the pixel data matrix is a square matrix having 2^n columns and 2^n rows of data elements.

26. An apparatus used in a display system that comprises an array of micromirrors, each micromirror being associated a memory cell of a memory cell array to produce images, the apparatus comprising:

a plurality of input lines that are associated with a sequence of time-units, each input line being designated for receiving a row of data elements of a pixel data matrix;

a delay unit connected to the plurality of input lines, wherein the delay unit delays the received data such that: a) a data element at input line j at time-unit k is delayed one time-unit relative to the data element at input line j at time-unit k+1; and b) the data element is delayed one time- unit relative to the data element at input line j-1 at time-unit k; and

a shifter connected to and receiving output data from the delay unit, wherein the shifter shifts the delayed data output from the first delay unit based on the sequence of time-units and according to a shifting rule, wherein the shifting rule states that:

a) the data element of line j at the k^{th} time-unit is shifted to line j-1 at the same time-unit; and the data element at line 1at the k^{th} time-unit is shifted to row m at the same time-unit, wherein k runs from 1 to $m+n$ time-units; and

b) the data elements at the n^{th} and m^{th} time-unit are not shifted.

27. The apparatus of claim 26, further comprises:

a shift register for shifting data elements at one time-unit.

28. The apparatus of claim 26, wherein the delay unit is a standard flipflop.

29. The apparatus of claim 26, wherein the delay unit is an aka shift register.

30. The apparatus of claim 26, wherein the number of data bits in each delay equals the number of data elements in the pixel matrix.

31. The apparatus of claim 26, wherein shift rule states that: the data element in the first row of the pixel data matrix, and the data element in the last row of the pixel matrix are not transposed thereby; and the data element between the first column and the last column of the pixel data matrix are to be permuted.

32. The apparatus of claim 26, wherein the input lines are connected to a plurality of input signals.

33. The apparatus of claim 32, wherein the input signals are data elements of a pixel data matrix.

34. The apparatus of claim 33, wherein the pixel data elements of the pixel data matrix is stored in a frame buffer to be loaded into a memory cell array.

35. The apparatus of claim 34, wherein the memory cell is a charge-pump-memory cell that further comprises:

a transistor having a source, a gate, and a drain;

a storage capacitor having a first plate and a second plate; and

wherein the source of said transistor is connected to a bitline, the gate of said transistor is connected to a wordline, and wherein the drain of the transistor is connected to the first plate of said storage capacitor forming a storage node, and wherein the second plate of said storage capacitor is connected to a pump signal.

36. The apparatus of claim 34, wherein the memory cell is a standard DRAM circuit.

37. The apparatus of claim 34, wherein the memory cell is a SRAM circuit.

38. The apparatus of claim 34, wherein each memory cell is connected to an addressing electrode.

39. The apparatus of claim 34, wherein the addressing electrode is associated with a mirror plate of the micromirror such that an electrostatic field is established between the mirror plate and the electrode.

40. The apparatus of claim 34, wherein the electrostatic field drives the mirror plate to rotate relative to the substrate.

41. An apparatus used in a display system that comprises an array of micromirrors, each micromirror being associated a memory cell of a memory cell array to produce images, the apparatus comprising:

a plurality of input lines that are associated with a sequence of time-units, each input line being designated for receiving a row of data elements of a pixel data matrix having m columns and n rows;

a multiplicity of sets of delay units, a) wherein a delay unit of the first set of delay units delays a data element one time-unit, and the delay units of the first set are connected to every two input lines, and b) wherein a delay unit of the s^{th} set of delay unit delays a data 2^{s-1} time-units, and the delay units of the s^{th} set are connected to every 2^{s-1} input lines;

a plurality of sets of switches, a)wherein a switch of the first set of switches exchanges data elements between input lines $2w$-1 and $2w$ with s running from 1 to $n/2$; and b) wherein a switch of the s^{th} set of switches exchanges data elements between $2w$-1 and $(n/2)+s$; and

wherein each switch of the s^{th} set of switches are located between and connected to two delay units of the s^{th} set of delay units.

42. The apparatus of claim 41, further comprising:

a shift register for shifting data elements at a time-unit.

43. An apparatus used in a display system that comprises an array of micromirrors for producing an image, the apparatus comprising:

a first input line and a second input line that are associated with a sequence of time-units for receiving data elements;

a first delay unit that is connected to the second input line and delays the received data element one time-unit;

a switch that is connected to the first input line and the first delay unit and receives data element from the output of the first delay unit, wherein the switch switches data elements between the first input line and the delayed data element output from the first delay unit; and

a second delay unit that is connected to the first input line and delays the received data element one time-unit.

44. The apparatus of claim 43, wherein the value of the data element determines the voltage of a memory cell of the memory cell array, and the time the data being received by the input line is associated with the duration of the voltage in the memory cell.

45. The apparatus of claim 43, further comprising:

a first output line that is connected to and receives output data from the second delay unit, and a second output line that is connected to the second input line; and

wherein the first output line and the second output line output data element to the memory cell of the memory cell array for actuating the micromirrors of the micromirror array.

46. The apparatus of claim 43, further comprising:

a shift register for shifting data at a time-unit.

47. The apparatus of claim 43, wherein each time unit of the sequence of time units is a clock cycle of the display system.

48. The apparatus of claim 43, wherein each time unit of the sequence of time units is a clock cycle of the display system.

49. The apparatus of claim 43, wherein the delay unit is a standard flipflop circuit.

50. The apparatus of claim 43, wherein the delay is a register.

51. The apparatus of claim 43, wherein the switch comprises a multiplexer.

52. The apparatus of claim 51, wherein the multiplexer is connected to and controlled by a control signal.

53. The apparatus of claim 52, wherein the control signal is associated with the sequence of time unit.

54. The apparatus of claim 44, wherein the memory cell is a standard SDRAM.

55. The apparatus of claim 44, wherein the memory cell is a charge-pump-memory-cell that further comprises:

a transistor having a source, a gate, and a drain;

a storage capacitor having a first plate and a second plate; and

wherein the source of said transistor is connected to a bitline, the gate of said transistor is connected to a wordline, and wherein the drain of the transistor is connected to the first plate of said storage capacitor forming a storage node, and wherein the second plate of said storage capacitor is connected to a pump signal.

56. The apparatus of claim 44, wherein the memory cell is part of a micromirror that further comprises a movable mirror plate.

57. The apparatus of claim 56, wherein the mirror plate is movable in response to an electrostatic field established between the mirror plate and an electrode that is connected to the memory cell, wherein the strength of the electrostatic field is determined by the voltage of the memory cell.

58. The apparatus of claim 57, wherein the micromirror represents a pixel of an image.

59. The apparatus of claim 46, further comprising: a frame buffer for storing the output data from the output lines.

60. The apparatus of claim 59, further comprising: a data processor that receives a stream of analog signals of an image and outputs a stream of pixel data corresponding to the stream of analog signals of the image.